

In re Patent Application of:
BORGATTI ET AL.
Serial No. 10/768,401
Filing Date: JANUARY 30, 2004

REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. Applicants would also like to thank the Examiner for correctly indicating as allowable the subject matter of dependent Claims 18, 27 and 36. The arguments supporting patentability of the claims are provided below.

I. The Claims

The present invention, as recited in independent device Claim 10, for example, is directed to a dynamically reconfigurable processing unit comprising a microprocessor, and an embedded Flash memory for non-volatile storage of code, data and bit-streams. The embedded Flash memory comprises a field programmable gate array (FPGA) port. The dynamically reconfigurable processing unit further comprises a direct memory access (DMA) channel, and an S-RAM embedded FPGA for FPGA reconfigurations. The S-RAM embedded FPGA comprises an FPGA programming interface connected to the FPGA port of the embedded Flash memory through the DMA channel. The microprocessor, the embedded Flash memory, the DMA channel and the S-RAM embedded FPGA are integrated as a single chip.

Independent device Claim 19 is similar to independent device Claim 10, but further recites a system bus connected between the microprocessor and the embedded Flash memory. Independent method Claim 28 is directed to a method for making a reconfigurable processing unit as defined in independent device Claim 10.

II. The Claims Are Patentable

Independent Claims 10, 19 and 28 were rejected over

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the Iwata et al. patent in view of the Helbig, Sr. et al. patent. The Examiner cited the Iwata et al. patent as disclosing a processing unit 1 in FIG. 1 as comprising a microprocessor 3, an embedded Flash memory 5 comprising a port, a direct memory access (DMA) channel 7, and an embedded SRAM 6.

As correctly noted by the Examiner, the Iwata et al. patent fails to disclose that the embedded SRAM 6 is connected to the port of the embedded Flash memory 5 via the DMA channel 7. The Examiner cited the Helbig, Sr. et al. patent as disclosing in FIG. 1 a Flash memory 30 comprising a port connected to a FPGA 38 and an SRAM 26 connected to a Flash memory 28.

However, the Examiner correctly notes that the FPGA 38 in the Helbig, Sr. et al. patent is not connected to the FPGA port of the Flash memory 28 through a DMA channel. The Examiner has taken the position that it would have been obvious to one of ordinary skill in the art at the time of the invention to make such a connection in the Iwata et al. patent to load the Flash memory from an external memory.

The Applicants submit that even if the references were combined as suggested by the Examiner, the claimed invention is still not produced. To produce the claimed invention, further modification is required to the Iwata et al. patent and/or the Helbig, Sr. et al. patent. Neither of the prior art references disclose connecting the FPGA to a Flash memory through a DMA channel. If it was obvious to do so as stated by the Examiner, then why hasn't such a connection been made?

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The Applicants respectfully submit that the Examiner is using impermissible hindsight reconstruction in an attempt to produce the claimed invention since neither of the references disclose the FPGA connected to the port of a Flash memory through a DMA channel. Accordingly, it is submitted that independent Claim 10 is patentable over the Iwata et al. patent in view of the Helbig, Sr. et al. patent.

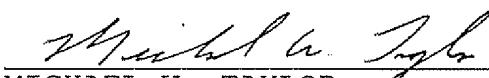
Independent Claims 19 and 28 are similar to independent Claim 10. Therefore, it is submitted that these claims are also patentable over the Iwata et al. patent in view of the Helbig, Sr. et al. patent. In view of the patentability of independent Claims 10, 19 and 28, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

III. CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

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Respectfully submitted,


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